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APPARATUS FOR PROVIDING TELEVISION RECEIVER ALIGNMENT FUNCTIONS

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This application claims the benefit of U.S. provisional application serial no. 60/102,429 filed September 30, 1998, which is hereby incorporated herein by reference.

BACKGROUND OF THE DISCLOSURE

1. Field of the Invention

The invention relates to television receivers and, more particularly, the invention relates to television receivers having a system microprocessor and a bus interface that facilitate a plurality of controllable functions for aligning the signals within the receiver.

BACKGROUND OF THE INVENTION

In modern television receivers, a microprocessor provides command and control information through an I^2C bus interface to provide various control functions. The I^2C bus is coupled to a module (an IF integrated circuit) comprising a tuner, IF, and stereo decoder. To achieve the best picture and sound performance, the microprocessor may have to control 8 or more alignment functions and various switch functions through the I^2C bus interface. These functions provide factory alignment of various signal characteristics such as video output amplitude and DC level, RF AGC delay threshold, and the like. Such electronic alignment is performed to ensure that a consistent picture quality between televisions occurs in retail show rooms; to ensure that consistent picture equality results between inputs of a television with multiple tuners or multiple auxiliary inputs; and to maintain signal levels within dynamic range limitations of the receiver circuitry.

There is a need in the television receiver art for an economical solution that enables a system microprocessor

to control a plurality of functions of the receiver to achieve accurate signal alignment.

SUMMARY OF THE INVENTION

The present invention is a method and apparatus within a television receiver for electronically aligning signals within the receiver by controlling support circuitry for a module comprising a tuner, IF and a stereo decoder. The invention uses a digital-to-analog converter (DAC) integrated circuit to control a plurality of alignment and switching functions within a television receiver. In one embodiment of the invention, a system microprocessor is coupled through an I^2C bus to a DAC that controls both video alignment and picture IF (PIF) mute functions. The DAC output is coupled to both a PIF mute circuit that in turn controls the IF AGC, i.e., switches the IF AGC off or on. The DAC is also coupled to a video level control circuit that controls the IF AGC gain. Using a six bit control signal, the microprocessor can control both the video level as well as the PIF mute circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

The teachings of the present invention can be readily understood by considering the following detailed description in conjunction with the accompanying drawings, in which:

FIG. 1 depicts a portion of a television receiver that is arranged in accordance with the present invention;

FIG. 2 depicts a schematic circuit of a PIF mute circuit;

FIG. 3 depicts a graph of the control voltage (DAC value) versus the PIF mute output;

FIG. 4 is a schematic diagram of the video level control circuit;

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FIG. 5A is a graphical depiction of an output signal of the video level control circuit for relatively low DAC values;

FIG. 5B is a graphical depiction of an output signal of the video level control circuit for relatively high DAC values;

FIG. 6 is a graph of the control voltage (Vc) versus video output level for the circuit of FIG. 5;

FIG. 7 is a schematic diagram of a video amplifier; and

FIG. 8 is a graph of the control voltage (DAC value) versus sync-tip level produced by the video amplifier of FIG. 7.

To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures.

DETAILED DESCRIPTION

FIG. 1 depicts a block diagram of a portion 100 of a television receiver comprising a signal processing module 106 as well as components of the present invention that support the operation of the module. The signal processing module 106 is, for example, a model LA7577N module manufactured by Sanyo Corporation. The module 106 comprises an IF circuitry for both sound (SIF) and picture (PIF). The audio circuitry portion 154 of the module 106 comprises an SIF amplifier 146 and SIF AGC 148, down converter 147 (mixer), a limiting amplifier 150 and an FM detector 152. Supporting the audio circuitry 154 is a 4.5 MHz bandpass filter 108. The audio circuitry 154, although it is a part of the television receiver module 106, forms no part of the present invention.

The video portion 156 of the module 106 comprises a PIF amplifier 134, a video detector 132, a phase detector 130, a voltage controlled oscillator (VCO) 140, an internal video amplifier 138, an equalization amplifier 144, an Nyquist slope canceller 142, an APC switch 128, a

lock detector 124, and IF AGC circuit 126 and an RF AGC amplifier 122. Supporting the video portion 156 of the module 106 is a PIF saw filter 102, a phase lock loop filter 104, a PIF AGC filter 118 and an external video amplifier 120 at the output of the module 106, as well as a sound trap 110 and a video level circuit 112. The IF video input is coupled to the PIF SAW filter 102 that filters the video signal. The SAW filtered video is amplified in IF amplifier 134, then down converted to baseband using the mixer 132. The mixer 132 is driven by the voltage controlled oscillator (VCO) 140. The baseband video is amplified by internal video amplifier 138. The amplified signal is filtered by the sound trap 110 and applied to the input of the video level control circuit 112. The operation of the video level control circuit 112 affects the IF AGC 126 which in affects the gain of the PIF Amp 134 and, thus, the video signal amplitude. The output of the video level control circuit 112 is applied to the equalization amplifier 144. The output of the equalization amplifier 144 is further amplified by video amplifier 120 to form the video output signal. The output of the PIF AGC filter is coupled to the lock detector 124 that drives the APC switch 128. The APC switch 128 selects the mode of operation for the PLL loop filter, i.e., whether the filter is operated in broad band mode (used during signal acquisition) or narrow band mode (used after PLL lock). The system microprocessor 158 couples digital control signals to DAC 114 that, in turn, controls the operation of both the level circuit 112 and the PIF mute 116.

It is important to note that the video level circuit is within the IF AGC loop and the IF amplifier gain is set by detecting the sync-tip level. As such, a change in the DC level of the video signal, as performed by the level circuit 112, changes the sync-tip level and the IF AGC loop gain. Consequently, a change in DC level controls the amplitude of the video signal.

The invention supports the module 106 through video level circuit 112 and PIF mute circuit 116, and an integrated circuit 160 containing a plurality (eight) digital-to-analog converters. In accordance with the present invention, a single DAC 114 within the integrated circuit 160 is used to control both the video level control circuit 112 and the PIF mute circuit 116. The DACs 160 are controlled by the system microprocessor 158 via the system I^2C serial bus 162.

The specific interconnections shown in FIG. 1 are representative of the interconnections within the LA7577N module 106. Those skilled in the art will realize that the inventive use of a digital-to-analog converter for controlling both the video alignment and the PIF mute functions could be used with many other arrangements of PIF circuitry. Similarly, the inventive video amplifier 120 and video level circuit 112 described below could be used in many other video processing applications.

The DAC 114 operates using 6 bits of input digital information to provide a variable analog output which is used to control both the PIF mute circuit 116 and the video level circuit 112. Alternatively, the DAC output, or the output of another DAC or other control voltage source, can be used to control the external video amplifier 120 (described below with respect to FIGS. 7 and 8). With respect to the invention, the system microprocessor, the I^2C bus and DAC or DACs collectively form a control voltage source or sources (collectively identified as reference number 160).

A DAC 114 that fulfills the functions of the present invention is a TDA 8444 manufactured by Phillips Corporation; however, other DACs and or control voltage generation circuits could be used. The output of the DAC 114 is coupled to the video level control circuit 112. This circuit is in essence a DC level shifter that sets the input DC level of the video signal into the equalization amplifier 144 of the module 106. The

accuracy of this DC level into the equalization amplifier is critical for proper operation of the video processing circuits down stream from the video amplifier 120 as well as to achieve proper operation of the IF AGC circuit. In the present invention less than six bits of the digital information are used for controlling the video DC level which is sufficient for the LA7577N. More or less bits could be used for other applications as those skilled in the art would easily understand. The same output from the DAC 114 that is coupled to the video level circuit 112 is also coupled to a PIF mute circuit 116.

The PIF mute circuit 116 sets the IF amplifier gain to minimum by pulling the IF AGC control voltage to ground. This function is used in the factory and field service to align the VCO free run frequency. In television receivers with auxiliary inputs, the PIF mute circuit 116 can also be used, if necessary, to prevent cross talk from the tuner IF video signal to the selected auxiliary input signal. In the present invention, the PIF mute function also sets the tuner RF amplifier gain to minimum because the RF AGC control voltage (pin 10) of module 106 is pulled to ground when the IF AGC control voltage is pulled below the reference voltage determined by the RF AGC delay alignment. This results in more effective muting than if only the IF amplifier is set to a minimum gain.

Using the circuitry described above, a single DAC 114 can be used for two functions if the two functions are a) complimentary or b) never used at the same time, but, when used, do not interfere with one another. Complimentary functions are those that are intended to be used at the same time. The video alignment and PIF mute functions are complimentary because a) the PIF mute must be deactivated whenever the video output must be set to the proper alignment point; and b) it is the intent to minimize the video output whenever the PIF mute is active. As such, a single DAC 114 can be used to control both the PIF mute circuit 116 and the video level circuit 112.

FIG. 2 depicts a schematic diagram of the PIF mute circuit 116. The output of the DAC 114 is coupled to the base of transistor Q203. This transistor has an emitter coupled to V_{ref} through resistor R200 and the collector of transistor Q203 is coupled to ground through resistor R202. The collector is also coupled to the base of transistor Q210 which forms a common emitter circuit having the collector coupled to a power supply through resistor R204. The collector of transistor Q210 is coupled through resistor R208 and to the base of transistor Q212.

The emitter of Q208 is pulled up to the reference voltage that sets the PIF mute switch point to approximately 1 V_{BE} below the maximum DAC output voltage. This guarantees switch operation using less than 1 bit of DAC range, while preserving as much DAC range as possible for video DC level control. The DAC output voltage is minimum when the DAC input value is 0 and maximum when the DAC input value is 63.

FIG. 3 depicts a typical characteristic curve 300 representing operation of the PIF mute circuit 116. The horizontal axis 302 depicts the control voltage (digital DAC values ranging from 0 to 63) and the PIF mute output voltage is shown on the right axis 304. For best understanding of the invention, FIGs. 2 and 3 should be referred to simultaneously. For DAC values less than 53, transistor Q212 is off and the PIF mute output voltage is determined by the IF AGC loop. At this DAC level, the DAC only controls the video DC level (as described below). For DAC values greater than or equal to 53, transistor Q212 is on and the PIF mute output pulls the AGC control signal to ground and the video output of the module 106 is minimized. While the video output is muted, the VCO free-run frequency is adjusted and the auxiliary inputs can be tested.

FIG. 4 depicts an embodiment of a video level circuit 112 of FIG. 1. This circuit 112 can be used in a television receiver arrangement described above, where a

single DAC 114 drives both the PIF mute circuit 116 and the video level control circuit or it can be used in a more traditional setting where the video level control circuit 112 is controlled by its own control voltage source.

In FIG. 4, transistors Q300 and Q302 isolate the DC level shift circuit 322 from the 4.5 Mhz soundtrap (110 in FIG. 1). Transistor Q300 is used to offset the V_{BE} drop of transistor Q302 which also minimizes temperature drift of the circuit 112. The DC voltage at the emitter of transistor Q302 is constant and the collector is coupled to ground through resistor R308. Therefore the DC level shift between Q302 emitter and the AGC detector input at pin 19 of module 106 of FIG. 1 depends on the value of R310 and the DC current determined by the current source comprising transistor Q304 and resistor R312. The current is controlled by voltage Vc, the output of a DAC, connected to R316. Capacitor C320 filters any noise that may be present at the DAC output.

The effectiveness of the circuit 112 is depicted in FIG. 6 wherein the control voltage (digital DAC values) are shown on the horizontal axis 600 and the video output values are shown on the left axis 602. As the DAC values increase, the video output amplitude (shown as curve 604) linearly decreases. Such an amplitude decrease occurs because the circuit 112 shifts the DC level of the video. This video level shift shifts the sync-tip level that is used to set the IF AGC gain. Consequently, the IF AGC circuit alters the gain of the IF amplifier (134 in FIG. 1). Typical factory alignment levels are superimposed upon the graph as horizontal dashed lines 6060 (upper level) and 608 (lower level). FIG. 5A depicts a video output signal from module 106 having a relatively low control voltage (less current through resistor R314) and FIG. 5B depicts a video output signal from module 106 having a relatively high control voltage (more current through resistor R314). Clearly, a change in the control voltage of the level circuit 112 effectively varies the

video signal amplitude. While the circuit shown in FIG. 4 was designed specifically for the LA7577N, the concept may be applied to other IF AGC integrated circuits where the DC level can be adjusted ahead of the AGC detector.

The present invention provides circuitry that facilitates television receiver signal alignment using a system microprocessor to control the alignment operation through the system I^2C bus. The circuitry includes a PIF mute circuit and a video level circuit. The PIF mute circuit and the video level circuit can be controlled by a single control voltage source. As such, the inventive circuitry provides additional signal alignment functionality during factory alignment and testing through the television receiver system's existing microprocessor and I^2C bus.

Although various embodiments which incorporate the teachings of the present invention have been shown and described in detail herein, those skilled in the art can readily devise many other varied embodiments that still incorporate these teachings.